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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/801,812	02/14/1997	JOHN H. GIVENS	11675.106	6774

22901 7590 09/12/2002

JESUS JUANOS I TIMONEDA
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UT 84111

EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	08/801,812	GIVENS, JOHN H.
	Examiner	Art Unit
	Julio J. Maldonado	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 24 July 2002.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 and 36-63 is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5)☐ Claim(s) ____ is/are allowed.

6)☒ Claim(s) 1-28 and 36-63 is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on ____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. ____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). ____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The final rejection as set forth in paper No. 25 is withdrawn in response to applicants' amendments.

2. A new 103(a) rejection is made as set forth in this Office Action.

3. Claims 1-28 and 36-63 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-5, 7-11 and 36-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu et al. (U.S. 5,847,461) in view of Xu et al. (Xu et al.', U.S. 6,217,721).

Xu et al. (Figs.1-4) in a related method to form an interconnect teach forming a recess (14) within a dielectric material (10) situated on a semiconductor lower substrate (2), wherein said recess (14) extends below a top surface (12) of said dielectric material (10); forming a diffusion barrier layer (20) comprising titanium nitride on the recess (14) within the dielectric material (10); forming an electrically conductive layer (30) comprising aluminum on the barrier layer (20), wherein the diffusion barrier layer (20) has a melting point greater than that of the electrically conductive layer (30); forming an energy absorbing layer (40) on said electrically conductive layer (30), wherein said energy absorbing layer (40) has a greater thermal absorption capacity than that of said

electrically conductive layer (30) and wherein said energy absorbing layer (40) is selected from the group consisting of titanium, tungsten, silicon dioxide and tantalum; using a furnace to apply energy omnidirectionally to said energy absorbing layer (40) causing said electrically conductive layer (30) to flow within said recess (14); and removing portions of the energy absorbing layer (40) and the electrically conductive layer (30) that are situated above the top surface of the dielectric material (10) (column 3, line 12 – column 7, line 45).

Xu et al. fail to teach the steps of heating the diffusion barrier layer in an environment substantially containing nitrogen gas; forming a seed layer comprising titanium nitride on the diffusion barrier layer, wherein the diffusion barrier layer has a melting point greater than or equal to the seed layer; forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, wherein the seed layer has a melting point greater than or equal to that the electrically conductive layer.

However, Xu et al.' (Fig.8) in a related method to form an interconnect teach the steps of heating a diffusion barrier layer (162) in an environment substantially containing nitrogen gas; forming a seed layer (164) comprising titanium nitride on a diffusion barrier layer (164), wherein the diffusion barrier layer (164) has a melting point greater than or equal to that of the seed layer (164); and forming an electrically conductive layer (156) on the seed layer (164) including the portion of the seed layer (164) within a recess (152), wherein the seed layer (164) has a melting point greater than or equal to that of the electrically conductive layer (156) (column 3, line 65 – column 6, line 45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a seed layer after the formation of the barrier layer and prior to the formation of the conductive layer, and having the thermal properties as taught by Xu et al.' in the interconnect formation method of Xu et al., since heating the barrier layer in a nitrogen environment substantially reduces the electronic barrier at the metal-semiconductor interface (column 9, lines 39-45) and the addition of titanium nitride as a seed layer improves the flow of aluminum into an interconnect at moderate temperatures (column 6, lines 40-45).

6. Claims 2, 6 and 12-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Xu et al. ('461) in view of Xu et al. (Xu et al.', '721) as applied to claims 1, 3-5, 7-11 and 36- 45 above, and further in view of Yim (U.S. 5,869,395).

Xu et al. in combination with Xu al.' substantially teach all aspects of the invention but fail to teach that the diffusion barrier layer and the seed layer are deposited on the recess by a chemical vapor deposition process; that a chemical-mechanical polishing is used to remove portions of the energy absorbing layer and the electrically conductive layer; that the recess has an aspect ratio greater that about four to one; and that the recess comprises a contact hole situated below a trench, wherein said semiconductor substrate has a lower substrate and terminates at an opposite end thereof at said trench, and wherein said trench extends from said opposite end of said contact hole to a top surface of said dielectric material and parallel to the plane of the lower substrate.

However, Yim (Figs.2A-2K) in a related method to form an interconnect structure teaches the steps of depositing titanium nitride by a chemical vapor deposition process; using chemical-mechanical polishing to remove portions overlaying a damascene trench formed on a dielectric layer (210); providing a recess comprising a contact hole (260) situated below a trench (240); providing a semiconductor substrate (200) having a lower substrate (202) and terminating at an opposite end thereof at said trench (240), wherein said trench (240) extends from said opposite end of said contact hole (260) to a top surface of said dielectric material (210), and parallel to the plane of the lower substrate (202) (column 4, line 26 – column 7, line 31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to deposit titanium nitride by chemical vapor deposition, using chemical mechanical polish to remove portions of conductive material overlying the dielectric layer and forming a recess comprising a trench and a contact hole as taught by Yim in the interconnect method of Xu et al. and Xu et al.', since this would result in a damascene opening with an alignment tolerance, reduced processing time and a flat topography (column 3, line 49 – column 4, line 5).

Still, the combination of Xu et al. Xu et al.' and Yim fail to teach that the recess has an aspect ratio greater than about four to one. However, the selection of the claimed range is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general

conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

7. Claims 16-28 and 57-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu et al. ('461) in view of Xu et al. (Xu et al.', '721) and Yim ('395).

Xu et al. (Figs.1-4) in a related method to form an interconnect teach patterning and etching a dielectric material (10) comprising silicon oxide situated on a semiconductor substrate assembly (2) so as to form a recess (14) within the dielectric material (10); depositing a diffusion barrier layer (20) comprising titanium nitride within the recess (14) within the dielectric material (10); depositing an electrically conductive layer (30) comprising aluminum on the barrier layer (20) within said recess (14), wherein the diffusion barrier layer (20) has a melting point greater than that of the electrically conductive layer (30); depositing an energy absorbing layer (40) on said electrically conductive layer (30), wherein said energy absorbing layer (40) has a greater thermal absorption capacity than that of said electrically conductive layer (30) and wherein said energy absorbing layer (40) is selected from the group consisting of titanium, tungsten, silicon dioxide and tantalum; using a furnace to heat omnidirectionally the energy absorbing layer, causing said conductive layer (30) to flow within said recess (14); and removing portions of the energy absorbing layer (40) and the electrically conductive layer (30) that are situated above the top surface of the dielectric material (10) (column 3, line 12 – column 7, line 45).

Xu et al. fail to teach the steps of heating the diffusion barrier layer in an environment substantially containing nitrogen gas; forming a seed layer comprising

titanium nitride on the diffusion barrier layer, wherein the diffusion barrier layer has a melting point greater than or equal to that of the seed layer; forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, wherein the seed layer has a melting point greater than or equal to that of the electrically conductive layer.

However, Xu et al.' (Fig.8) in a related method to form an interconnect teach the steps of heating a diffusion barrier layer (162) in an environment substantially containing nitrogen gas; forming a seed layer (164) comprising titanium nitride on a diffusion barrier layer (164), wherein the diffusion barrier layer (164) has a melting point greater than or equal to that of the seed layer (164); and forming an electrically conductive layer (156) on the seed layer (164) including the portion of the seed layer (164) within a recess (152), wherein the seed layer (164) is composed has a melting point greater than or equal to that of the electrically conductive layer (156) (column 3, line 65 – column 6, line 45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a seed layer after the formation of the barrier layer and prior to the formation of the conductive layer and having the thermal properties as taught by Xu et al.' in the interconnect formation method of Xu et al., since heating the barrier layer in a nitrogen environment substantially reduces the electronic barrier at the metal-semiconductor interface (column 9, lines 39-45) and the addition of titanium nitride as a seed layer improves the flow of aluminum into an interconnect at moderate temperatures (column 6, lines 40-45).

Still, the combination of Xu et al. and Xu al.' fail to teach using chemical-mechanical polishing to remove portions of the energy absorbing layer and the electrically conductive layer; and providing a recess comprising a contact hole situated below a trench, wherein said semiconductor substrate has a lower substrate and terminates at an opposite end thereof at said trench, wherein said trench extends from said opposite end of said contact hole to a top surface of said dielectric material and parallel to the plane of the lower substrate. However, Yim (Figs.2A-2K) in a related method to form an interconnect structure teaches the steps of using chemical-mechanical polishing to remove portions overlaying a damascene trench formed on a dielectric layer (210); providing a recess comprising a contact hole (260) situated below a trench (240); providing a semiconductor substrate (200) having a lower substrate (202) and terminating at an opposite end thereof at said trench (240), wherein said trench (240) extends from said opposite end of said contact hole (260) to a top surface of said dielectric material (210) and parallel to the plane of the lower substrate (202) (column 4, line 26 – column 7, line 31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use chemical mechanical polish to remove portions of conductive material overlying the dielectric layer and forming a recess comprising a trench and a contact hole as taught by Yim in the interconnect method of Xu et al. and Xu et al.', since this would result in a damascene opening with an alignment tolerance, reduced processing time and a flat topography (column 3, line 49 – column 4, line 5).

8. Claims 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu et al. ('461) in view of Yim ('395).

Xu et al. in a related method to form an interconnect teach the steps of forming a dielectric material (10) over a semiconductor substrate (2) and having a top surface; forming a recess (14) within the dielectric material (10) extending from the top surface of the dielectric material (10) to the semiconductor substrate (2); filling the recess (14) with an electrically conductive material (30), wherein filling the recess (14) is performed by causing the electrically conductive material (30) to flow within the recess (14) by applying omnidirectional heating (column 3, line 12 – column 7, line 45).

Xu et al. fail to provide a recess including a first portion having an uniform width and extending within the dielectric material to the top surface of the dielectric material and a second portion having a height and a uniform width that is less than the width of the first portion and that is not greater than 25% of the height, wherein the second portion extends from the semiconductor substrate to terminate at the first portion, and wherein the first portion is a trench having a bottom surface that extends longitudinally parallel to the top surface of the dielectric material, and that the second portion is a contact plug.

However, Yim (Figs.2A-2K) provide a recess including a first portion (240) having an uniform width and extending within the dielectric material (210) to the top surface of the dielectric material (210) and a second portion (260) having a height and a uniform width that is less than the width of the first portion (240), wherein the second portion (260) extends from the semiconductor substrate (202) to terminate at the first portion

(240), and wherein the first portion (240) is a trench having a bottom surface that extends longitudinally parallel to the top surface of the dielectric material (210), and that the second portion (260) is a contact plug. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a recess comprising a trench and a contact hole as taught by Yim in the interconnect method of Xu et al., since this would result in a damascene opening with an alignment tolerance, reduced processing time and a flat topography (column 3, line 49 – column 4, line 5).

Still, the combination of Xu et al. Xu et al.' and Yim fail to teach that and that the width of the first portion is not greater than 25% of the height. However, the selection of the claimed range is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

9. Claims 48-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu et al. ('461) in view of Yim ('395) as applied to claims 46 and 47 above, and further in view of Xu et al. (Xu et al.', '721).

Xu et al. in combination with Yim teach forming a diffusion barrier layer comprising titanium nitride on the recess in contact with the semiconductor substrate and the dielectric material; forming a conductor layer comprising aluminum upon the barrier layer, wherein the diffusion barrier layer has a melting point greater than that of the electrically conductive layer; forming an energy absorbing layer on said electrically

conductive layer, wherein said energy absorbing layer has a greater thermal absorption capacity than that of said electrically conductive layer and wherein said energy absorbing layer is selected from the group consisting of titanium, tungsten, silicon dioxide and tantalum; and performing said omnidirectional heating on a furnace applying, (Xu et al., column 3, line 12 – column 7, line 45).

Xu et al. in combination with Yim fail to teach the steps forming a seed layer comprising titanium nitride on the diffusion barrier layer, wherein the diffusion barrier layer has a melting point greater than or equal to that of the seed layer; and forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, wherein the seed layer has a melting point greater than or equal to that of the electrically conductive layer is composed.

However, Xu et al.' (Fig.8) in a related method to form an interconnect teach the steps of forming a seed layer (164) comprising titanium nitride on a diffusion barrier layer (164), wherein the diffusion barrier layer (164) has a melting point greater than or equal to that of the seed layer (164); and forming an electrically conductive layer (156) on the seed layer (164) including the portion of the seed layer (164) within a recess (152), wherein the seed layer (164) has a melting point greater than or equal to that of the electrically conductive layer (156) (column 3, line 65 – column 6, line 45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a seed layer after the formation of the barrier layer and prior to the formation of the conductive layer having the thermal properties as taught by Xu et al.' in the interconnect formation method of Xu et al. and Yim, since the

addition of titanium nitride as a seed layer improves the flow of aluminum into an interconnect at moderate temperatures (column 6, lines 40-45).

Response to Arguments

10. Applicant's arguments with respect to claims 1-28 and 36-63 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

703-306-0098
julio.maldonado@uspto.gov

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800